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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,044	02/09/2004	Randall S. Mundt	AWS-040	8988
25199	7590	10/03/2005	EXAMINER	
LARRY WILLIAMS 3645 MONTGOMERY DR SANTA ROSA, CA 95405-5212			LAU, TUNG S	
			ART UNIT	PAPER NUMBER
			2863	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/775,044

Applicant(s)

MUNDT, RANDALL S.

Examiner

Tung S. Lau

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 15 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 3,5 and 16-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5, 22-38, 16, 17 is/are allowed.
- 6) ☒ Claim(s) 3 and 18-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

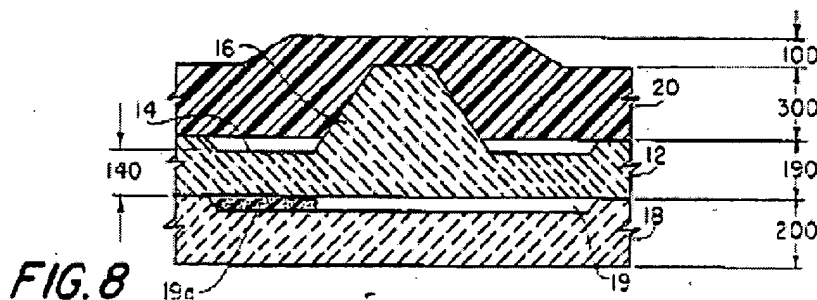
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3 and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Amazeen et al. (U.S. Patent 4,745,812).

Regarding claim 3:

Amazeen discloses a process tolerant sensor apparatus comprising:

a bottom substrate (fig. 8, unit 18); b) a top substrate (fig. 8, unit 12, 20); c) a plurality of sensors disposed between the bottom substrate and the top substrate (Col. 5-6, Lines 6-2);



d) a plurality of electrically conductive interconnects disposed between the bottom substrate and the top substrate (Col. 5-6, Lines 6-2); e) electrically active components connected to the conductive interconnects for at least one of data acquisition, data storage, and communications; and bonding material

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substantially filling the volume between the bottom substrate and the top substrate (Col. 6-7, Lines 3-32), wherein the top substrate comprises a silicon wafer (Col. 5, Lines 38-41).

Regarding claim 18:

Amazeen discloses in a combination: a bottom semiconductor wafer (fig. 8, unit 18); a top semiconductor wafer (fig. 8, unit 12, 20); a plurality of sensors disposed between the bottom semiconductor wafer and the top semiconductor wafer (Col. 5-6, Lines 6-2);; a plurality of electrically conductive interconnects disposed between the bottom semiconductor wafer and the top semiconductor wafer (Col. 5-6, Lines 6-2); an electronics module comprising a housing containing electrically active components connected to the conductive interconnects for at least one of data acquisition, data storage (Col. 6-7, Lines 3-32), and communication; and a bonding material substantially filling the volume between the bottom semiconductor wafer and the top semiconductor wafer (Col. 6-7, Lines 3-32).

Regarding claim 19, Amazeen discloses the top semiconductor wafer having a hole for receiving at least a portion of the electronics module (fig. 8, unit 12);

Regarding claim 20, Amazeen discloses the top semiconductor wafer having a layer of electromagnetic field shielding material (Col. 5-6, Lines 60-2); Regarding claim 21, Amazeen discloses bottom substrate is a silicon wafer (Col. 5, Lines 51-59);

***Allowable Subject Matter***

2. Claims 5, 22-38, 16, 17 are allowed.

***Reasons for Allowance***

3. The following is an examiner's statement of reasons for allowance:

Independent claims 5, 16 and 17 contain allowable subject matter. None of the prior art of record shows or fairly suggests the claimed invention.

Regarding claims 5, 16 and 17:

Please see previous office action and applicant's response filed on 09/15/2005 for reason for allowance.

Claims 22-38 are allowed due to their dependency on claim 5.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Response to Arguments***

4. Applicant's arguments filed 09/15/2005 have been fully considered but they are not persuasive.

A. Applicant argues in the arguments that the prior art does not show the 'the combination of a bottom semiconductor wafer, a top semiconductor wafer, and a plurality of sensors disposed between the bottom semiconductor wafer and the top semiconductor wafer', and that the applicant compare the Amazeen invention to the applicant.

Amazeen discloses 'the combination of a bottom semiconductor wafer (fig. 8, unit 18), a top semiconductor wafer (fig. 8, unit 12), and a plurality of sensors disposed between the bottom semiconductor wafer and the top semiconductor wafer (Col. 5-6, Lines 6-2, abstract); As regards to applicant compare the Amazeen invention to the applicant's invention, the examiner reminds to the applicants that during patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification." Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969). While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allowed. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

**B.** Applicant continues to argue in the arguments that the prior art does not show the structure of the applicant as taught by the applicant. Amazeen discloses the claims structure in claims 3 and 18. Reminds to the applicant that while the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allowed. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

**C.** Applicant continues to argue in the arguments that the prior art does not show 'a top substrate comprising a semiconductor wafer, a bottom substrate, and a plurality of sensors between the top substrate and the bottom substrate'. Amazeen discloses 'a top substrate comprising a semiconductor wafer (fig. 8, unit 12, Col. 5, Lines 37-40), a bottom substrate (fig. 8, unit 18), and a plurality of sensors between the top substrate and the bottom substrate (Col. 5-6, Lines 6-2)'.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed

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within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). TL

**BRYAN BUI**  
**PRIMARY EXAMINER**



9/29/05